SECTION A –Amendments to the claims:

Claim 1. (currently amended):

A photonic-electronic multiple-layer circuit package family having electrical intra-layer and electrical inter-layer interconnection means, optical intra-layer and optical inter-layer interconnection means, plus ~~electronic~~ electrical and optical escape means, and including electronic and optical transducer means both intra-layer and inter-layer

characterized by:

an electrical interconnected pattern layer having a selected pattern for connectivity to operational elements, and having physical gaps appropriately positioned for optical vias; and

optical inter-layer interconnection via means positioned for unobstructed optical passage through intervening layers at said gaps in the electrical interconnect pattern.

2. (currently amended):

A photonic-electronic multiple-layer circuit package family ~~according to Claim 1,~~ in which ~~said~~ optical via gaps are arrayed in a standard matrix pattern having electrical intra-layer and electrical inter-layer interconnection means, optical intra-layer and optical inter-layer interconnection means, plus electrical and optical escape means; and including electronic and optical transducer means both intra-layer and inter-layer

characterized by:

an electrical interconnected pattern layer having a selected pattern for connectivity to operational elements, and having physical gaps appropriately positioned for optical vias; and

optical inter-layer interconnection via means, in which said optical via gaps are arrayed in a standard matrix pattern, positioned for unobstructed optical passage through intervening layers at said gaps in the electrical interconnect pattern.

3. (original) :

A photonic-electronic multiple-layer circuit package family according to Claim 2, in which said optical via gaps are arrayed in a selected pattern appropriate for a selected photonic-electronic configuration.

4. (currently amended):

A photonic-electronic multiple-layer circuit package family having electrical intra-layer and electrical inter-layer interconnection means, optical intra-layer and optical inter-layer interconnection means, plus electronic and optical escape means, and including electronic and optical transducer means both intra-layer and inter-layer

characterized by:

an electrical interconnected pattern layer having a selected pattern for connectivity to operational elements, and having physical gaps appropriately positioned for optical vias; and

optical inter-layer interconnection via means, with embedded photonic bandgap devices, in which said optical via gaps are arrayed in a standard matrix pattern, positioned for unobstructed optical passage through intervening layers at said gaps in the electrical interconnect pattern.

5 (currently amended):

A photonic-electronic multiple-layer circuit package according to Claim 2, with embedded diffractive elemental modulators. [devices.]

6. (canceled)

A photonic-electronic multiple-layer circuit package according to Claim 2, with embedded diffractive elemental modulator devices.

7. (original)

A photonic-electronic multiple-layer circuit package according to Claim 2, with at least one of the following optical devices included:

optical clock, optical transceiver, detector arrays, waveguides, splitters, taps, switches, filters, wavelength multiplexers, wavelength demultiplexers, interconnected by optical switching and routing means; and

interconnected electronic circuitry and power circuitry.

8. (original) :

A photonic-electronic multiple-layer circuit package according to Claim 1, with multiple layers aligned together

further characterized in that

said multiple aligned layers are subject to alignment anomalies; and

said optical vias and said electrical vias are aligned with accommodation for such alignment anomalies and for noninterference.

9. (original) :

A photonic-electronic multiple-layer circuit package according to Claim 1, with integral rounded optical waveguides for low-loss connectivity to individually aligned rounded optical fibers.

10. (allowed)

A photonic-electronic multiple-layer circuit in which said integral rounded optical waveguides are produced by depositing and pattern-etching a thick layer of a first TIR-complementary photoresist over a first TIR-complementary base material, to form a TIR-complementary rounded-bottom half channel corresponding to the bottom half of an optical fiber to be connected; depositing an optical waveguide material over said photoresist and half channel to a thickness which, combined with the thickness of said first photoresist, approximates the diameter of the optical fiber to be connected; patterning a central channel mask of a second photoresist material over said optical waveguide material, centered above said half channel so that etching will result in rounding the top of the optical waveguide material; etching away said optical waveguide material down to said first photoresist, and removing said second photoresist, to leave a half-embedded half-exposed rounded waveguide approximating an optical fiber; and covering said photoresist layer and said rounded waveguide material with a TIR-complementary material, so as to complete the TIR encapsulation of said waveguide material and leave effectively rounded TIR waveguides ready for low-loss connection to rounded optical fibers.

11. (allowed)

A photonic-electronic multiple-layer printed circuit package according to Claim 10, in which said integral rounded optical waveguides are half embedded in a thick layer of a photoresist over a first TIR-complementary base material, to form a rounded-bottom half channel corresponding to the bottom half of an optical fiber to be connected;

an optical waveguide material over said half channel to a thickness which, combined with the thickness of said photoresist, approximates the diameter of the optical fiber to be connected,

a TIR-complementary layer over said optical waveguide material, to leave a fully embedded rounded waveguide approximating in shape and dimension an optical fiber; covered with a TIR-complementary material, completing the encapsulation of said waveguide material and leaving effectively round waveguides ready for low-loss connection by butt joint to aligned flat ends of round optical fibers at a polished edge.

12. (allowed)

The method of making a photonic-electronic circuit package termination characterized as follows:

Step 1 Deposit, pattern, and develop a photoresist layer to leave a slope-sided run of photoresist over a base;

Step 2 Deposit waveguide material B filling said slope-sided run and over the remainder of said photoresist layer;

Step 3 Deposit protective mask layer D, of width related to the diameter of the desired rounded cross-section of waveguide, over said waveguide run; and

Step 4 Etch unwanted B down to layer A, leaving a waveguide run of material B of rounded cross-section, to approximate a ridge waveguide with rounded terminations.

13. (allowed)

The method of making a photonic-electronic circuit package termination according to Claim 12, further characterized as follows:

Step 5 Deposit overlayer C over said remaining waveguide run to approximate a channel waveguide with rounded terminations.

14. (allowed)

The method of Claim 12, in which the waveguide resulting at Step 4 is further characterized by:

Step 5. Apply photoresist layer, expose and develop a well at a selected angle transition;

Step 6. Deposit metal on side walls of said well, and strip resist;

Step 7. Apply photoresist layer R2, expose waveguide regions and etch all areas except waveguide regions, so that all non-waveguiding regions are exposed; and

Step 8a. Photobleach optically transmissive material so as to be lower in refractive index from said waveguide layer (101) material, forming a channel type waveguide.

15. (allowed)

A photonic-electronic waveguide circuit board with off-board connective provision, for contacting to optical fibers having rounded cross-section of a selected diameter,

characterized by:

a photonic printed circuit fabricated by the methods of Claim 13, in which a selected portion of the waveguide pattern resulting at Step 4 is further characterized by rounded cross-section fabricated as follows:

Step 5 Deposit overlayer C and grind the edge flat vertical, leaving a termination for a butt joint of round cross-section photonic printed circuit waveguide run with a flat distal end for accepting a mating flat distal end of a similar-dimensioned round optical fiber.

16. (allowed)

The method of making a photonic-electronic circuit package, in the following steps:

Step 1 Provide a composite layer of waveguide-forming material (C 11) with a complementary waveguide-forming material (A12) and a layer of photoresist (R1 13);

Step 2 Pattern and develop said photoresist layer (R1 13) into a turning pattern (14) for a waveguide layer (12);

Step 3 Remove sacrificial portion of waveguide layer (12) to leave patterned waveguide (15);

Step 4 Coat with overlayer (B 16) to leave a channel waveguide with a turning mirror right angle effectuated by total internal reflection.

17. (allowed)

The method of making a photonic-electronic circuit package, in the following steps:

Step 1 Provide a composite layer of waveguide-forming material (C 11) with a complementary waveguide-forming material (A12) and a layer of photoresist (R1 13);

Step 2 Image and develop to form a rectangular well (24) appropriately placed and angled for a turning mirror;

Step 3 Etch to transfer the well into the layer (A 12) to complete the well opening (25) stopping at the base layer (C 11);

Step 4 Metallize with a mirror layer (26) on walls of the well;

Step 5 Strip resist (R1 23), leaving mirrorized wall (27) in the well;

Step 6 Apply planarizing photoresist layer (R2 28), expose waveguide regions and etch all areas except waveguide regions, so that all non-waveguiding regions and desired mirror (30) are exposed, forming a ridge waveguide.

18. (allowed)

The method of making a photonic-electronic circuit package according to Claim 17, further characterized by

the planarizing photoresist (R2 29) is patterned with a small overhang to protect the mirror layer (30) under the overhang.

19. (allowed)

The method of making a photonic-electronic circuit package according to Claim 17, further characterized by

Step 7 Coat with a complementary TIR waveguide-forming layer (B 38) of lower refractive from said waveguide layer material, forming a channel-type waveguide of total internal reflection, except at metallized mirror facet transitions, to convert from ridge waveguide to channel waveguide.

20. (allowed)

The method of making a photonic-electronic circuit package according to Claim 17, further characterized by:

Step 7. Photobleach optically transmissive material so as to be lower in refractive index from said waveguide layer (A 12) material, forming a channel type waveguide.

21. (allowed)

The method of making a photonic circuit package according to Claim 17, further characterized by

the planarizing photoresist (R2 29) is patterned with a small overhang to protect the mirror layer (30) under the overhang.

22. (allowed)

The method of making a photonic circuit package according to Claim 17, further characterized by substitution of direct photoablation for photoresist techniques in making the non-waveguiding regions of said waveguide layer (12).

23. (allowed)

The method of making a photonic-electronic circuit package, in the following steps:

Step 1 Provide a composite layer of waveguide-forming material (C 11) with a layer of photoresist (R 41);

Step 2 Image and develop to form a pillar (42) appropriately placed and angled for a turning mirror, but having a set of undesired curves as well as a desired mirror base portion;

Step 3 Develop and bake to cure said pillar (42);

Step 4 Metallize with a mirror layer (43) on said pillar;

Step 5 Deposit underlayer (44) to cover at least one of said undesired curves of said pedestal (42); and

Step 6 Apply waveguide material layer over said underlayer, so that the waveguiding region addresses said desired mirror base portion of said pedestal (42) ; leaving a vertical light beam exit perpendicular to said waveguide material layer.

24. (allowed)

The method of making a photonic-electronic circuit package, according to Claim 23, further characterized in that said mirror layer is removed to be discontinuous just outside said waveguide layer under said underlayer (44).

25. (allowed)

The method of making a photonic-electronic circuit package, according to Claim 23, further characterized in that said mirror layer is removed to be discontinuous just outside said waveguide layer under both said underlayer (44) and said overcoat layer (B 46).

26. (allowed)

The method of making a photonic-electronic circuit package, according to Claim 23, further characterized by the following steps:

Step 7 Deposit a thick photoresist layer over a top portion of said pedestal (42);

Step 8 Expose and develop a well (52) ;

Step 9 Fill said well (52) with waveguide material (54): and

Step 10 Coat all around said waveguide material (54) with a lower refractive index waveguide complementary TIR material (53) to provide an vertical optical exit via.

27. (allowed)

The method of making a photonic-electronic circuit package, according to Claim 25, further characterized by the following steps:

Step 11 Coat with underlayer (C" 71) of optical material that obeys the condition $n_{C"} < n_{A.}$, pattern a gap and fill with waveguide material (A 72) as an extension vertical waveguide;

Step 12 Coat with waveguide material (A 73) and a top coating of material (B 74) and a thick layer of resist (R 62);

Step 13 Pattern and develop said thick layer of resist (R 62) with clearance past said vertical waveguide extension (72):

Step 14 Etch to transfer the slope into layers (71, 73 and 74) down to the leave of said vertical waveguide (54) and remove resist (R 62); and

Step 15 Coat with TIR waveguide-complementary material (B 76), resulting in a vertical optical via turning into a horizontal optical waveguide in a parallel layer.